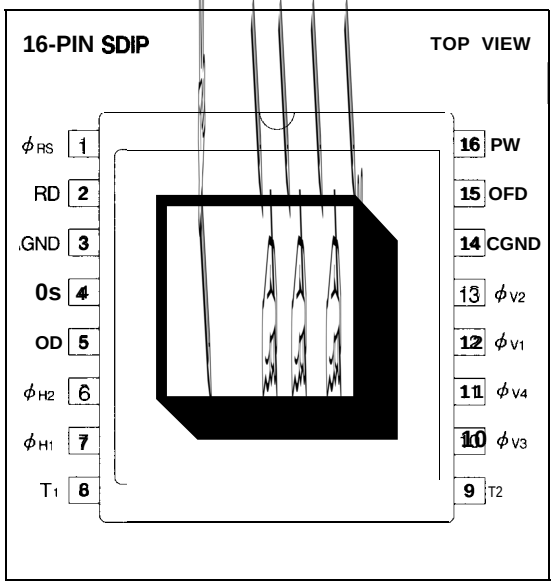
LZ2314J

1/3 type B/W **CCD** Area Sensor for EIA

DESCRIPTION

U2314J is a 1/3-type (6.0 mm) solid-state image sensor that consists of PN phote-diodes and CCDS (charge-coupled devices). Having approximately 270000 pixels (horizontal 542 x vertical 492), the sensor provides a high resolution stable B/W image,

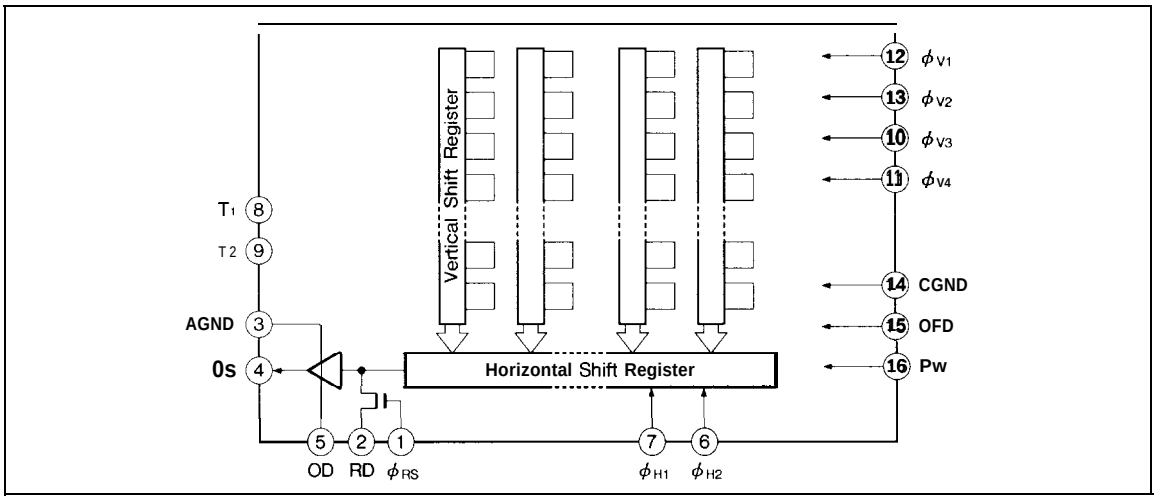
PIN CONNECTIONS



FEATURES

- **Number of pixels : 512 (H) x 492 (V)**
  Pixel pitch : 9.6 μm(H) × 7.5 μm (V)
  Number of optical black pixels
  : Horizontal; front 2 and rear 28
- **Low fixed pattern noise and lag**
- **No sticking and no image distortion**
- **Blooming suppression structure**
- **Built-in output amplifier**
- **Variable electronic shutter (1/60 to 1/10 000 s)**
- **Compatible with EIA standard**
- **Package : 16-pin SDIPICERDIP](WDIPO1 6-N-050( )**

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
RD	Reset transistor drain
OD	Output transistor drain
0s	Video output
ϕ_{RS}	Reset transistor gate clock
ϕ_{V1}, ϕ_{V2}, ϕ_{V3}, ϕ_{V4}	Vertical shift register gate clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register gate clock
OFD	Overflow drain
Pw	P type well
AGND	Analog part ground
CGND	Clock part ground
T_1, T_2	Test terminal

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Output transistor drain voltage	V_{OD}	Oto +18	v
Reset transistor drain voltage	V_{RD}	Oto +18	v
Overflow drain voltage	V_{OFD}	o to +55	v
Test terminal, T_1	V_{T1}	Oto +18	v
Test terminal, T_2	V_{T2}	–0.3 to +18	v
Reset gate clock voltage	$V_{\phi RS}$	–0.3 to +18	v
Vertical shift register clock voltage	$V_{\phi V}$	–9.0 to +18	v
Horizontal shift register clock voltage	$V_{\phi H}$	–0.3 to +18	v
Voltage difference between PW and vertical clock	$V_{PW} - V_{\phi V}$	–27 to O	v
Storage temperature	Tstg	–20 to +80	°C
Operating ambient temperature	Topr	–20 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		Topr		25,0		℃	
Output transistor drain voltage		V_{OD}	14.5	15.0	16.0	v	
Reset transistor drain voltage		V_{RD}		V_{OD}		v	
Overflow drain voltage	When DC is applied	V_{OFD}	5.0		19.0	v	1
	When pulse is applied p-p level	$V_{\phi OFD}$	22.0			v	2
Analog part ground		AGND		0.0		v	
Clock part ground		CGND		0.0		v	
P-well voltage		V_{PW}	-9.0		$V_{\phi VL}$	v	
Test terminal, T1		V_{T1}		V_{OD}		v	
Test terminal, T2		V_{T2}		0,0		v	
Vertical shift register clock	LOW level	$V_{\phi V1L}$, $V_{\phi V2L}$ $V_{\phi V3L}$, $V_{\phi V4L}$	-8.5	-8.0	-7,5	v	
	INTERMEDIATE level	$V_{\phi V1I}$, $V_{\phi V2I}$ $V_{\phi V3I}$, $V_{\phi V4I}$		0,0		v	
	HIGH level	$V_{\phi V1H}$, $V_{\phi V3H}$	16.0	16.5	17.0	v	
Horizontal shift register clock	LOW level	$V_{\phi H1L}$, $V_{\phi H2L}$	-0.05	0.0	0.05	v	
	HIGH level	$V_{\phi H1H}$, $V_{\phi H2H}$	4,7	5.0	6.0	v	
Reset gate clink	LOW level	$V_{\phi RSL}$	0,0		$V_{RD}-12.0$	v	
	HIGH level	$V_{\phi RSH}$	$V_{RD}-7.5$		9.5	v	
Vertical shift register clock frequency		$f_{\phi V1}$, $f_{\phi V2}$ $f_{\phi V3}$, $f_{\phi V4}$		15.73		kHz	
Horizontal shift register clock frequency		$f_{\phi H1}$, $f_{\phi H2}$		9.53		MHz	
Reset gate clock frequency		$f_{\phi RS}$		9.53		MHz	

NOTES :

1. When DC voltage is applied, shutter speed is 1 /60 seconds.
2. When pulse is applied, shutter spaed is less than 1/60 seconds.

ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

(Ta= 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

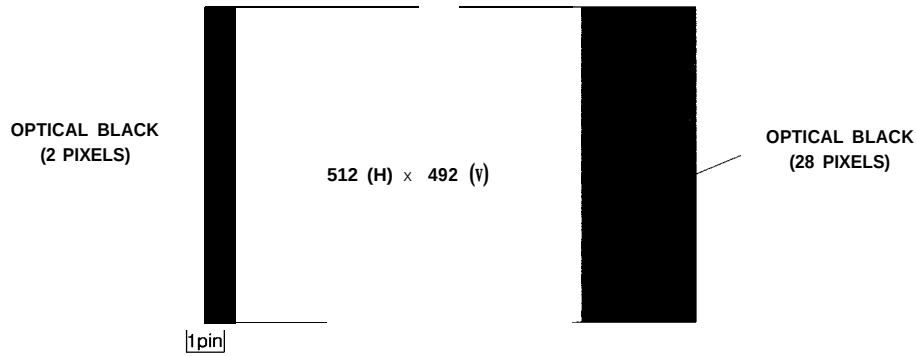
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Photo response non-uniformity	PRNU			10	%	2
Saturation signal	Vsat	500			mV	3
Dark output voltage	Vdark		0.3	3.0	mV	1, 4
Dark signal non-uniformity	DSNU		0.6	2.0	mV	1, 5
Sensitivity	R	240	360		mV	6
Gamma	Y		1			
Smear ratio	SMR		0.009	0,016	%	7
Image lag	Al			1.0	%	8
Blooming suppression ratio	ABL	1000				9
Output transistor drain current	I_{OD}		4.0	6.0	mA	
Output impedance	R_O		300		Ω	
Dark noise	Vnoise		0,2	0.4	mV	10
OB difference in level				1,0	mV	11

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

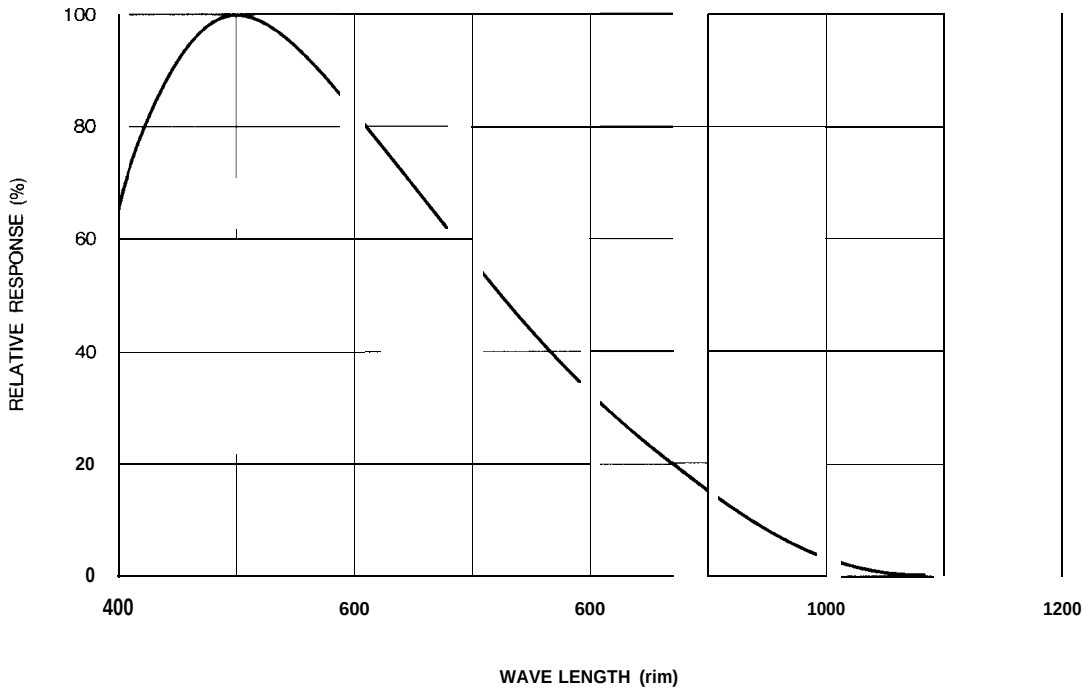
NOTES :

1. Ta : +60°C
2. The image area is divided into 10X 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage Vo is 150 mV.
3. The image area is divided into 10X 10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average output voltage of allthe pixels within the segment, when the exposure level is set as 10 times, compared to standard level.
4. The average output voltage under a non-exposure condition.
5. The image area is divided into 10X 10 segments. DSNU is defined by (Vdmax – Vdmin) under the non-exposure condition where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
6. The average output voltage when a 1 000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
7. The sensor is adjusted to position a V/l O square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/l O square.
8. The sensor is exposed at the exposure level corresoonding to the standard condition preceding non-exposure condition. Al is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
9. The sensor is adjusted to position a V/l O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
10. The RMS value of the dark noise (after CDS). The bandwidth range is from 1 00 kHz to 4.2 MHz.
11. The difference between the average output voltage of the effective area and the OB part under the non-exposure condition.

PIXEL STRUCTURE



SPECTRAL RESPONSE EXAMPLE

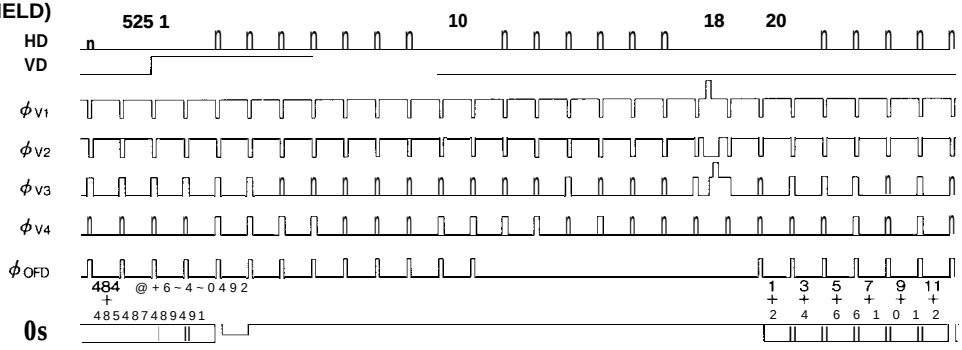


TIMING DIAGRAM EXAMPLE

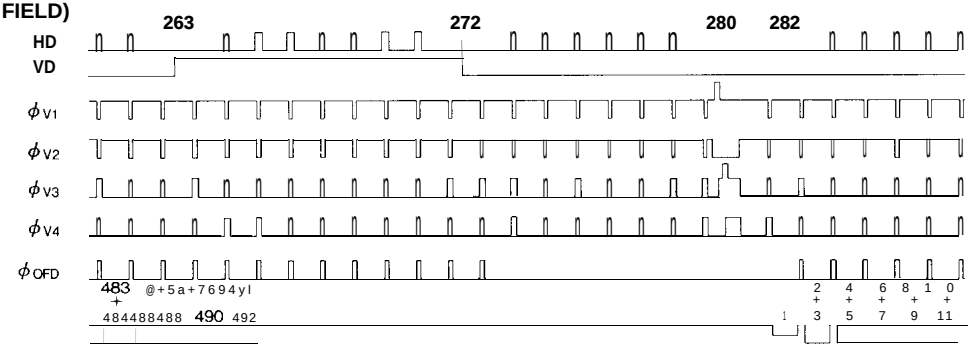
VERTICAL TRANSFER TIMING

Shutter speed 1/2000 s

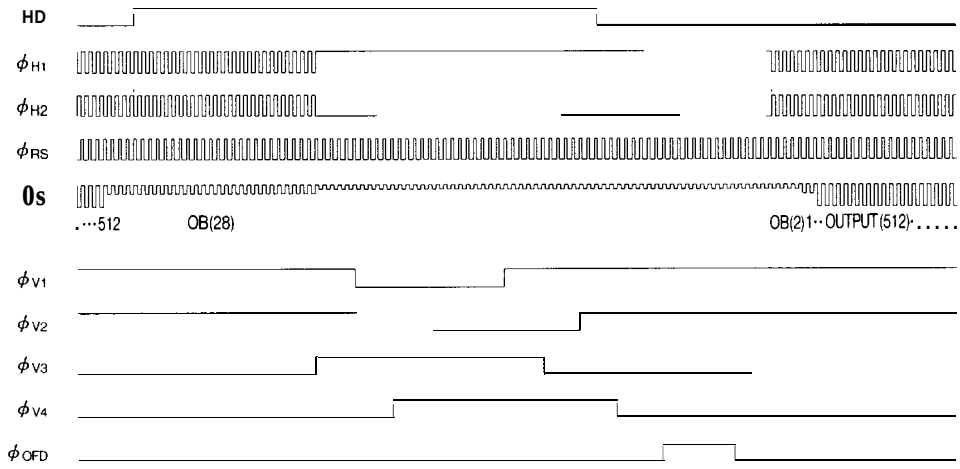
(ODD FIELD)



(EVEN FIELD)

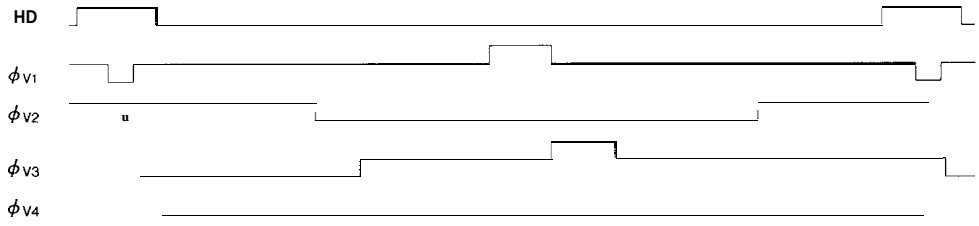


HORIZONTAL TRANSFER TIMING

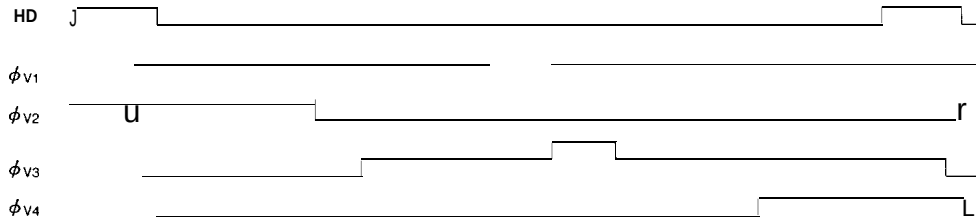


READOUT TIMING

(ODD FIELD)



(EVEN FIELD)



SYSTEM CONFIGURATION EXAMPLE